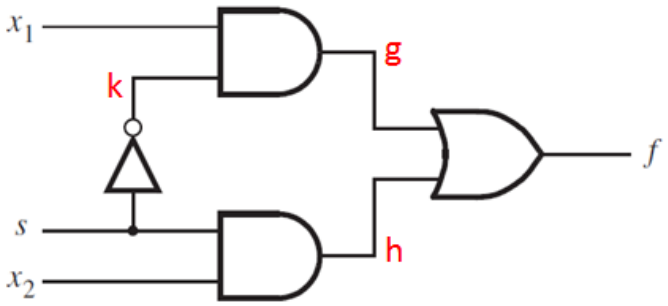
BEE 271 Spring 2017
Homework 3

Please answer the following questions. Each is worth 10 points.

1. What's the difference between a reg and a wire? If a variable isn't defined in Verilog, what does it default to?
2. What is a vector in Verilog? If it's not a vector, what is it?
3. What does { 2{ 4'h3 }, 2'b1 } equal? What is the { … } operation called?
4. What does this circuit do? Is there a name for it? Write it as a Verilog module using only built-in gates and give it an appropriate name.




5. Write the same function as a Verilog module using continuous assignment.
6. Write the same function as a Verilog module as a behavioral specification.
7. What are three different ways to represent signed numbers in binary? Which method is commonly used, why is it preferred and how is it calculated?
8. What is the difference between carryout and overflow?
9. What's the difference between a half-adder and a full-adder? Draw the truth table and gate-level schematic for a full adder.
10. What is critical path delay?